Design of Low Power VLSI Circuits using Energy Efficient Adiabatic Logic

Amit Shukla, Arvind Kumar, Abhishek Rai and S.P. Singh

Abstract—In this paper, a new design of adiabatic circuit, called energy efficient adiabatic logic (EEAL) is proposed. Earlier various diode based adiabatic logic families have been proposed. To achieve minimum energy consumption, this paper proposes a technique in which diode is replaced by MOS transistor at charging and discharging path whose gate is controlled by the power clocks. By using this technique non adiabatic loss and power consumption of the diode is eliminated. In the proposed circuit, the input and output logic levels are nearly the same and can be used for building cascaded logic circuits. The split level sinusoidal power supply is used to achieve low power high speed adiabatic circuits. In this paper we have designed and simulated NOT, NAND, NOR gates, Half Adder and Full adder circuit. All simulations in this paper have been implemented by VIRTUOSO SPECTRE simulator of cadence with the 0.18 µm UMC technology MOS transistor model under 1.8-volt peak to peak split level sinusoidal power clock supply. From the simulation result, we find that proposed logic circuits can save significant amount of energy compared to CMOS circuits and GFCAL circuits with similar parameters up to 500MHz.

Index Terms— Adiabatic logic, Energy efficient, Low power, Power delay product, Power dissipation, Recovery logic, Split level power clock

- *Amit Shukla,Abhishek Rai and S.P.Singh are with the Department of Electronice and Communication engg. (VLSI Design) MNNIT Allahabad India (corresponding author email amitshukla33@gmail.com)*
- *Arvind kumar is Asst. Professor with the Department of Electronics and Communication engg. MNNIT Allahabad India(email arvindk@mnnit.ac.in)*

1 INTRODUCTION

Demands for low power electronics have motivated designers to explore new approaches to VLSI circuits. The classical approaches of reducing power consumption in conventional CMOS circuits included reducing the supply voltages, node capacitances, and switching frequencies. The power consumption in conventional CMOS is proportional to the square of the power supply voltage; therefore, voltage scaling is one of the important methods used to reduce power consumption. To achieve a high transistor drive current and improve the circuit performance, the transistor threshold voltage (V_t) must be scaled down in proportion to the supply voltage. However, scaling down of the transistor threshold voltage (V_t) results in proportional increase in subthreshold leakage current [1].

Adiabatic systems have been applied to low power devices. Various adiabatic logic families have been proposed [2-15] emphasizing on the energy recovery principle. There are two types of adiabatic circuits; fully adiabatic and quasi adiabatic circuits. Fully adiabatic circuits are more complex then quasi adiabatic circuits, and hence not grown in popularity as quasi adiabatic circuits, which have simpler architecture and power supply [2].

Fully adiabatic circuits suffer from adiabatic loss due to the leakage current through non-ideal switches. Quasi-adiabatic circuits suffer from adiabatic and non-adiabatic loss. Non-adiabatic loss is proportional to the capacitance driven and square of the threshold voltage. Adiabatic loss is proportional to frequency but non-adiabatic loss is independent on frequency. The term 'adiabatic' means reversible thermodynamic process where a transformation takes place in such a way that no gain or loss of energy occurs [3]. Some energy recovery logic has been proposed [4-7]. They have achieved significant energy saving compared with conventional logic but output of these circuits are valid only during a particular phase of power clock. Hence, multiple-phase clocking is required to drive a chain of cascaded adiabatic logic circuits. Younis and Knight have proposed adiabatic logic families with less dissipation but each gate requires 16 times the number of devices compared with conventional logic [8].Dickinson and Denker have used a diode based adiabatic dynamic logic circuits [9]. The drawbacks are that the gates are dynamic and require four phase clocking for cascading the gates. Antonio and Saletti proposed a positive feedback adiabatic logic gate, but this requires four phase power clock and requires the input in its complement form [10]. Recently diode based adiabatic logic circuits have been

proposed [11-15]. Most of them achieve significant power saving but they have several disadvantage such as output amplitude degradation, large delay, complex circuit structure and power dissipation across the diode in the charging path.

In this paper, we propose energy efficient adiabatic logic circuits. EEAL inherits all the advantages of recently reported adiabatic logic circuits with additional improvement in power saving. By using the EEAL circuits, we can achieve high output amplitudes and reduce power dissipation. To minimize the dynamic power consumption in this circuit, we apply a split level sinusoidal supply voltage. Further we have also proposed various EEAL based logic circuits and compare their performances with the recently reported (GFCAL) glitch free cascadeble adiabatic logic circuits and conventional CMOS circuit.

This paper is divided into five sections. Section 1 deals the introduction part. Section 2 describes the differences between conventional CMOS and adiabatic circuits. Section 3 describes the proposed energy efficient adiabatic logic (EEAL) circuit operation and its analysis. In section 4 discusses about EEAL based various circuit. Conclusion is given in the section 5.

2 Conventional CMOS Circuits Verses Adiabatic Logic Circuits

In conventional CMOS circuits, load capacitor (C) is charge from a dc power supply and discharging it to ground, whereas, in adiabatic circuits, the load capacitor is charge through the varying power supply and it discharge to the varying power supply instead of discharging it to ground. Power dissipation in logic circuits primarily occurs during switching. The inverter can be considered to consist of a pull-up (PMOS) and pull-down (NMOS) networks connected to the load capacitance (C). Both pull-up and pull-down networks can be modeled by an ideal switch in series with resistor (R) which is equal to corresponding channel resistance of the transistor. For understanding the charging and discharging process, inverter can be modeled as simple RC circuit.

2.2 Conventional Charging

Consider a simple RC circuit as shown in figure 1. Assume that initially the charge on the capacitor is 0 and it starts charging at time t =0 from constant power supply voltage V. At any instant of time the voltage on the capacitor is v(t). A small amount of charge dq to the capacitor requires an amount of work dW = v(t)dq. The total work done in charging the capacitor from 0 to Q coulombs is

$$W = \int_0^Q v(t)dq \qquad (1)$$

At any instant, the voltage across the capacitor $v(t) = \frac{q(t)}{C}$

So equation (1) becomes

$$W = \int_0^Q \frac{q(t)}{C} dq = \frac{1}{2} CV^2 \qquad (2)$$

The energy drawn from the power supply

$$E = QV = CV^2 \qquad (3)$$

So energy dissipated by resistor is during charging

$$E_{diss} = E - W = \frac{1}{2} CV^2 \qquad (4)$$

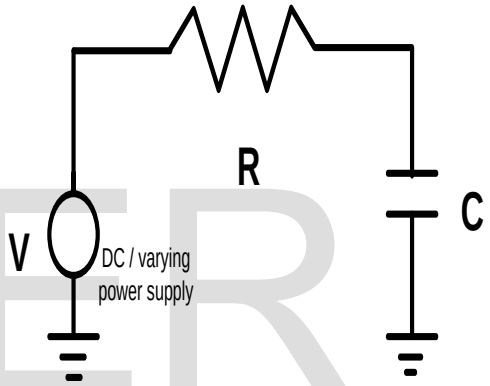


Figure 1 Simple RC circuit

This shows that one half of the energy is dissipated as heat during charging through pull-up networks (PMOS) and half of energy is stored in load capacitor. Hence in conventional CMOS, during a complete charge-discharge cycle, the energy CV^2 is withdrawn from power supply and is dissipated as heat. Half of this energy dissipated during charging and half of energy dissipated during discharging.

2.2 Adiabatic Charging

In adiabatic charging, capacitor is charge by the time varying power supply. For convenient we take ramp type voltage source $V(t) = \frac{V}{T}$, where V is the peak voltage of power supply and T is the time period. At any instant of time the current

$$i(t) = \frac{VC}{T}(1- e^{-t/RC}).$$

Energy dissipated across the resistor during charging

$$E_{diss} = \int_0^T i^2(t)Rdt \approx \left(\frac{RC}{T}\right) CV^2,$$

$$(T >> RC) \qquad (5)$$

Compare equation (4) & (5), it has been seen that if time period of charging/discharging T is much greater then RC, then energy dissipation in adiabatic is less than conventional CMOS. That is, energy dissipation can be made arbitrarily small by increasing the charging time T.

3 Proposed Energy Efficient Adiabatic Logic (EEAL) Inverter

3.1 Circuit Description

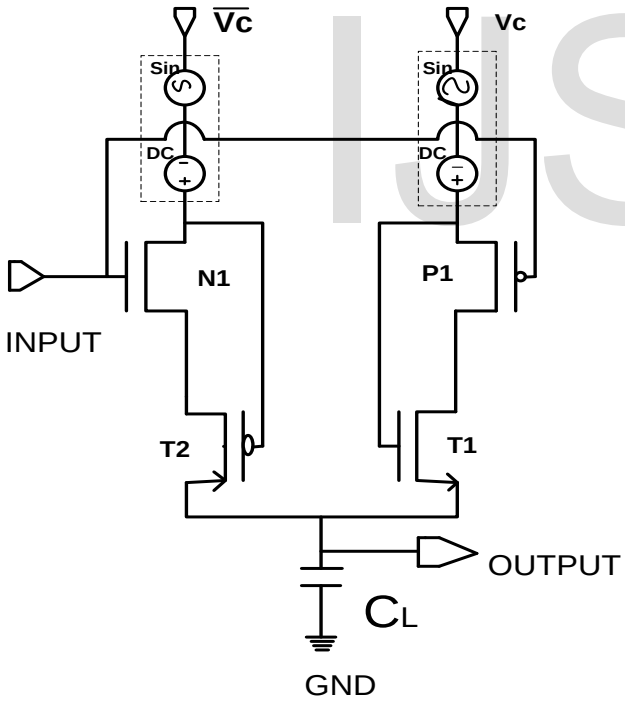


Figure 2(a) Proposed EEAL inverter circuits

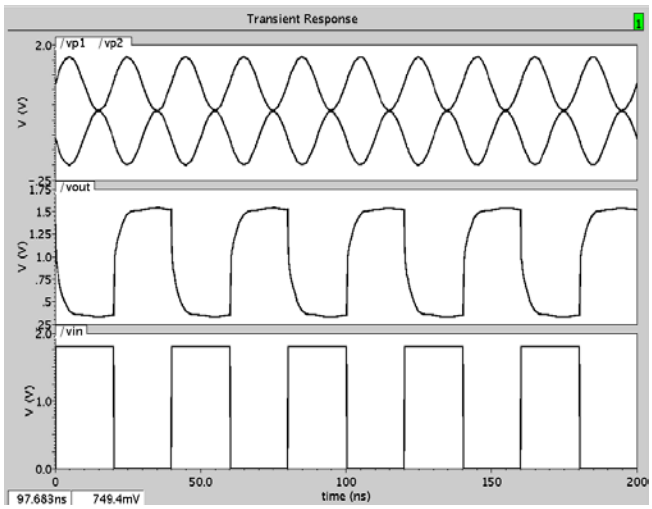


Figure 2(b) Proposed EEAL inverter simulation waveforms

The basic schematic of energy efficient adiabatic logic circuit is shown in fig. 2(a). This circuits involve an N-network, P-network and one charging NMOS transistor (T1) and one discharging PMOS (T2) whose gate are controlled by power supply. The EEAL circuits use two complementary split level sinusoidal power supply (Vc & $\overline{Vc}$). The voltage level of Vc exceeds that of $\overline{Vc}$ by a factor of $V_{dd}/2$. One power supply is in phase while other supply is out of phase which has peak-to-peak voltages of 1.8V in a 180nm CMOS process. The power supply design still meets the requirement in, where the voltage difference between current carrying electrodes must be zero when the transistor switches to the ON State. The power supply expression is given as follows:

$$V_C = \frac{V_{dd}}{4}\sin(\omega t + \theta) + \frac{3}{4}V_{dd}$$

$$\overline{Vc} = -\frac{V_{dd}}{4}\sin(\omega t + \theta) + \frac{1}{4}V_{dd}$$

The NMOS transistor (T1) is in the pull-up network and PMOS transistor (T2) in the pull-down network are use in the place of diode for the charging and discharging. At the charging and discharging path, channel resistance is same so, circuit is balanced. The power dissipation due to ON resistance is significantly lower than the power dissipation due to the threshold voltage drop through diodes. Hence using MOS transistor, power dissipation is reduced compare to the diode based adiabatic circuits. The simulated waveform of proposed inverter in fig 2(b) shows that logic level difference between input and output is very small and can be used for building cascaded logic circuits.

3.2 Circuit Operation

For understanding the circuit operation of proposed inverter, first let's assume that the output capacitor is initially uncharged state and input is logic '0'. In this case, the transistor P1 will be ON while the transistor N1 is OFF. When Vc is increasing and $\overline{Vc}$ decreasing, at some point where power supply Vc exceeds the threshold voltage Vtn of the transistor T1, the transistor T1 turns ON and starts charging the capacitor. So logic '0' gives logic '1' at the output.

When output capacitor is initially charged and input is logic '1'. In this case the transistor N1 will be ON while the transistor P1 is OFF, since the gate of the transistor T2 is connected to $\overline{Vc}$, the transistor T2 will ON at the point where the $\overline{Vc}$ exceeds the threshold voltage Vtp of that transistor. The output capacitor starts discharging. So logic '1' gives logic '0' at the output. Hence the output is the complement of the input.

When output capacitor is initially uncharged state and input is logic '1'. In this case the transistor N1 will be ON and transistor P1 will be OFF. At the discharging path transistor T2 will be OFF, this is because power clock does not exceed the threshold voltage Vtp of the transistor and thus prevents discharging. So the capacitor remains unchanged. Thus logic '1' gives logic '0' at the output.

When output capacitor is initially charged and input is logic '0'. In this case the transistor P1 will be ON and transistor N1 will be OFF. At the charging path transistor T1 will be OFF, this is because due to large threshold voltage Vtn of the transistor and thus prevents charging. So capacitor remains unchanged. Thus logic '0' gives logic '1' at the output.

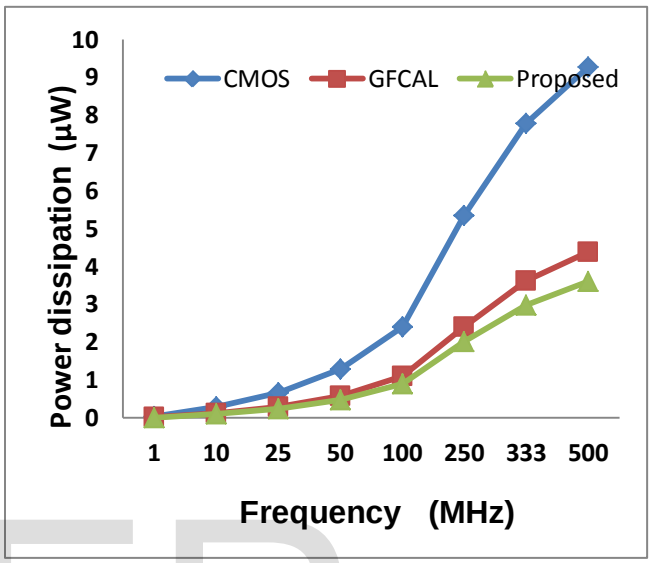
In last two cases, no transitions occur at the output so dynamic switching is reduce and thus energy dissipation is also reduce in proposed logic circuits.

3.3 Efficiency of proposed inverter circuit with frequency

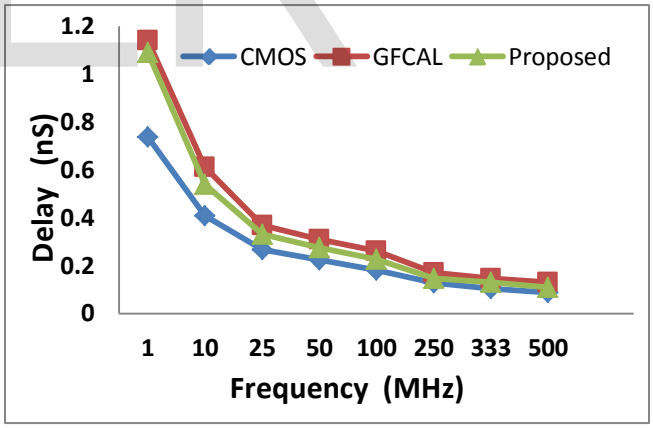
Here we check the performance of the Proposed EEAL, GFCAL and conventional CMOS inverter. The circuit of the inverter is simulated using VIRTUOSO SPECTRE circuit simulator of cadence EDA tools. The length and width of the transistor are 180 nm and 240 nm, respectively the value of load capacitance is 5 fF; we have been simulated their power and delay and compared with the variation in transition frequency.

3.4 Comparison of power, delay and PDP with frequency at fixed load capacitance

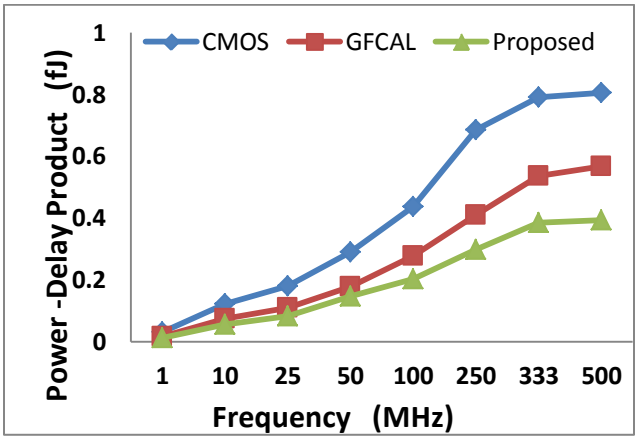
The input and supply frequencies are varied simultaneously from 1 MHz to 500 MHz. For better performance power supply frequency should be greater than two time of input supply frequency.



(a)



(b)



(c)

Figure 3 Simulation result of inverter compare in term of (a) Power dissipation with varying frequency, **(b)** Delay with varying frequency, **(c)** Power-delay-product with varying frequency

In the graph, we have seen that as input frequency increase, power dissipation of both the inverter increases whereas proposed (EEAL) inverter have lesser power dissipation at each frequency in comparison to conventional CMOS and GFCAL. The output logic levels up to frequencies of 50MHz are 1.65 V corresponding to logic '1' and 0.25 V corresponding to logic '0'. It has been observed that as frequencies increases then 50 MHz, the logic value corresponding '1' is decreases and logic value corresponding '0' is increases. At frequencies higher than 500 MHz, the difference between logic'1' and logic '0' becomes small. This is because the time period of the supply waveform is small compared with the time constant of charging and discharging, and the capacitor is unable to charge and discharge to the required levels. However a continuous decrease in delay for both the inverter with input frequency is observed. Initially proposed EEAL inverter has larger delay then conventional CMOS but less than GFCAL. When input frequency reaches around 50 MHz the difference between their delays are minimized. Thus from given observation it is observed that power efficiency and overall power delay product (PDP) is improved 50% in comparison to conventional CMOS and 20% in comparison to GFCAL throughout the whole frequency range.

3.5 Efficiency of proposed inverter circuits with load capacitance

Diode using MOS transistors are weak in driving capability. Here we observe the driving capability of the proposed EEAL inverter without using any diode; we simulate the proposed inverter by adding different one by one load capacitor at the output node. Input supply frequency kept 50 MHz and for better performance, power supply frequency kept 100 MHz. As the load capacitance takes time to charge or discharge based on its capacitance value, a large capacitance will lead to slow charging and discharging and small capacitance values give very fast charge and discharge times. However a disadvantage of using smaller capacitance is the ripple observed in the output waveform.

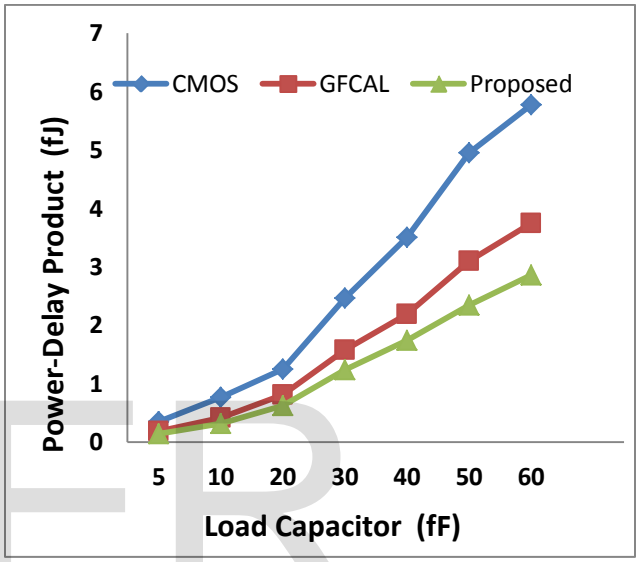


Figure 4 simulation result of inverter compare in term of PDP with varying load capacitor

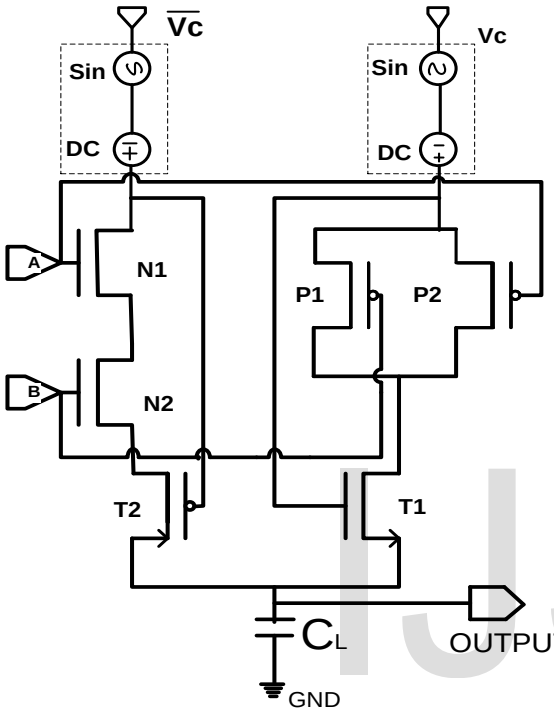
Here we observed that when load capacitance is increases the power dissipation of both inverters correspondingly increases but a very small delay increase in comparison to conventional CMOS but less than GFCAL. However our proposed EEAL inverter has better energy efficient than conventional CMOS at all load capacitor. From simulation result it is observed that power efficiency and overall power delay product (PDP) is significant improved in comparison to conventional CMOS and GFCAL throughout the all load capacitor.

4 Proposed EEAL based logic circuits

The NAND and NOR gates are universal gates and used to design complex digital circuits. As we cannot build adiabatic circuits by simply using conventional method therefore an optimized design of these gates can certainly benefit the performance of the larger circuits. In the

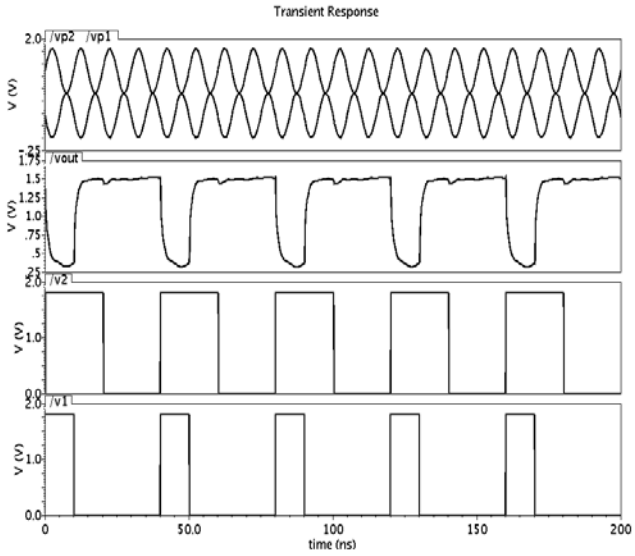
following subsections, various logic such as NAND, NOR, Half adder and Full adder circuits have been implemented based on proposed EEAL design. The simulation at 25 MHz is done by VIRTUOSO SPECTRE circuit simulator of cadence EDA tools. The length and width of the transistor are 180 nm and 240 nm.

4.1 Proposed EEAL NAND gate



(a)

Circuit diagram of proposed adiabatic NAND gate is shown in Fig 5(a). This circuit consists of two branches. The first branch consists of two parallel P-channels MOSFET (P1 & P2) and a N-channel MOSFET (T1) connected in series. The second branch consist of two series N-channel MOSFET (N1 & N2) and a P-channel MOSFET (T2) connected in series. The output of load capacitance is charged/discharged through charging/discharging (nMOS/pMOS) T1 & T2 whose gate is directly connected with split level sinusoidal power clock (V_c and $\overline{Vc}$). Gate of P1 & N1 are tied together with an input A and P2 & N2 with another input B.

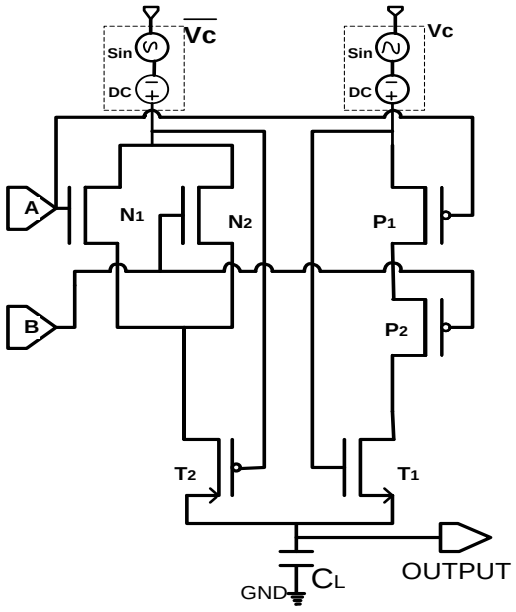


(b)

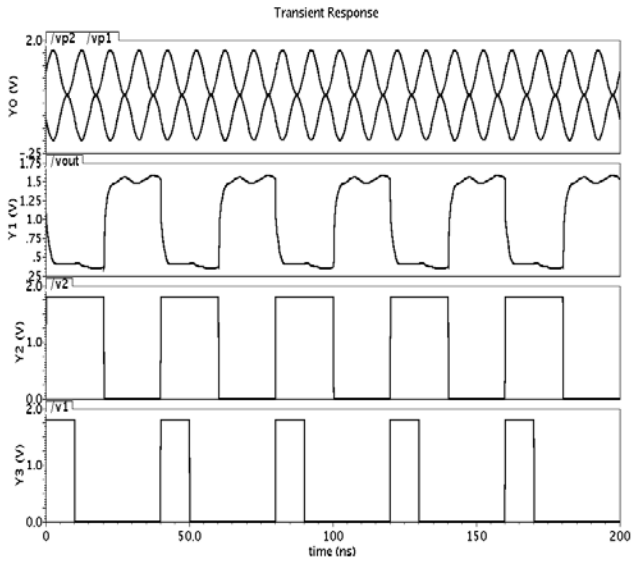
Figure 5 Proposed EEAL NAND logic gate (a) Circuit diagram, (b) Simulation waveform

The simulated timing waveforms for input string A = 10001000100010001000, B= 11001100110011001100 and output = 01110111011101110111 are shown in Fig 5(b). When any input has logic '0', then output give logic '1' otherwise output give logic '0'. Thus a NAND operation is realized. From the simulation result, it has been seen that the power dissipation in the proposed NAND gate is about 60% of that of a CMOS and about 15% of that of GFCAL NAND gates.

4.2 Proposed EEAL NOR gate



(a)



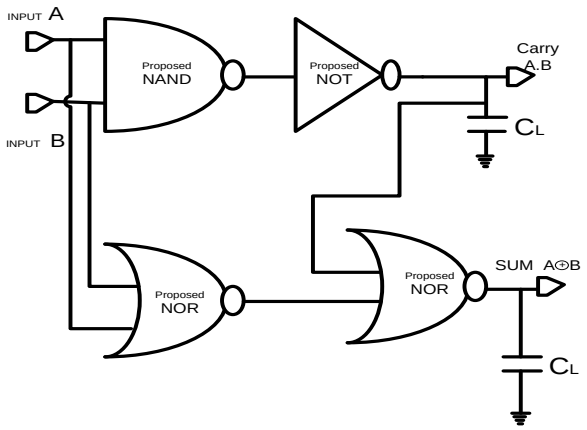
(b)

Figure 6 Proposed EEAL NOR logic gate (a) Circuit diagram, (b) Simulation waveform

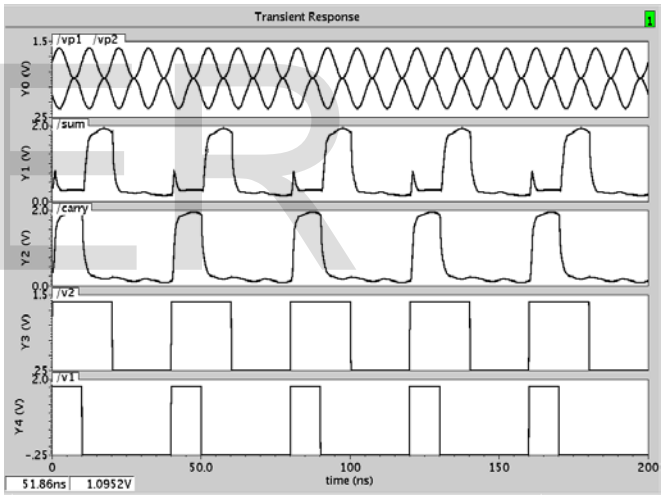
Circuit diagram of proposed adiabatic NOR gate is shown in Fig 6(a). This circuit consists of two branches. The first branch consists of two series P-channel MOSFET (P1 & P2) and a N-channel MOSFET (T1) connected in series. The second branch consists of two parallel N-channel MOSFET (N1 & N2) and a P-channel MOSFET (T2) connected in series. The output of load capacitance is charged/discharged through charging/discharging (nMOS/pMOS) T1 & T2 whose gate is directly connected with split level sinusoidal power clock (V_c and $\overline{Vc}$). Gate of P1 & N1 are tied together with an input A and P2 & N2 with another input B. The simulated timing waveforms for input string A = 10001000100010001000, B= 11001100110011001100 and output = 00110011001100110011 are shown in Fig 6(b). When any input has logic '1', then output give logic '0' otherwise output give logic '1'. Thus a NOR operation is realized. From the simulation result, it has been seen that the power dissipation in the proposed NOR gate is about 60% of that of a CMOS and about 15% of that of GFCAL NOR gates.

4.3 Proposed EEAL Half Adder

The half adder circuit is realized using two NOR gates and one AND gate as shown in Fig 7(a). The AND gate is realized by connecting the output of a NAND gate as input to the inverter. The OR gate is realized by connecting the output of a NOR gate as input to the inverter.



(a)



(b)

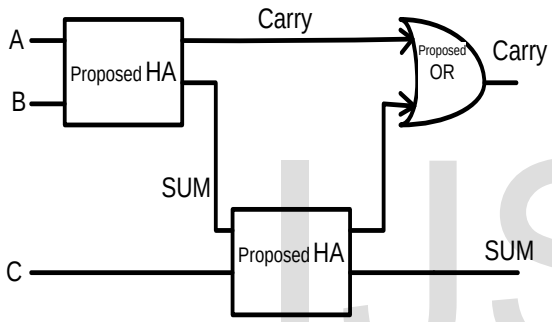
Figure 7 Proposed EEAL Half Adder (a) Block diagram, (b) Simulation waveform

In order to realize a operation, consider the truth table for half-adder. The outputs namely the SUM and CARRY .It is required that the SUM should be logic '0' when both inputs are same i.e logic 0. For the logic '1' output, the inputs can be any of the two combinations i.e. 01, 10, i.e input are not same. The CARRY is taken at the output node, which follow as the AND gate. The combination of inputs '00, 01, 10, 11' are given in the form of strings A = '10001000100010001000' and B = '11001100110011001100'. The outputs namely the SUM and CARRY are obtained as

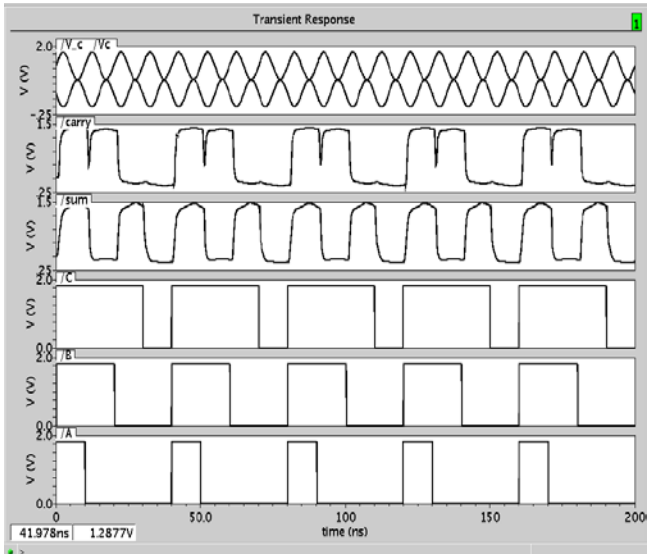
strings SUM ='01000100010001000100' and CARRY = '10001000100010001000', respectively. Simulated waveform is shown in Fig 7(b) at different input frequency. From the simulation result, it has been seen that CMOS half adder takes double power consumed by the proposed adiabatic half adder.

4.4 Proposed EEAL Full Adder

The Full adder circuit is realized using two half adders and an OR gate as shown in Fig 8 (a). The OR gate is realized by connecting the output of a NOR gate as a input of inverter. The supply for all the circuits is used split level sinusoidal power clock.



(a)



(b)

Figure 8 Proposed EEAL Full Adder (a) Block diagram, (b) Simulation waveform

The performance of full adder circuit is same as that of the half adder. Full adder has three input and output is SUM and CARRY. The combination of input for all state are given in the form of string A = '1000100010001000' B = '1100110011001100' and C = '1110111011101110'. The output namely the SUM and CARRY are obtained as strings SUM = '1010101010101010' and CARRY = '1100110011001100' respectively. Simulated waveform is shown in Fig 8(b) at different input frequency. For better performance, Power clock frequency should take more than two times of input frequency.

4.5 Comparison of power dissipation for the proposed EEAL full adder, GFCAL full adder and CMOS full adder at different transition frequency

Input Frequency	Power dissipation (µW) in Proposed full adder	Power dissipation (µW) in GFCAL full adder	Power dissipation (µW) in CMOS full adder
1 MHz	0.35	0.43	0.64
5MHz	1.21	1.41	2.12
10MHz	1.86	2.24	3.37
25MHz	4.34	5.96	7.76
50MHz	9.12	12.4	18.6
100MHz	15.3	18.8	28.5

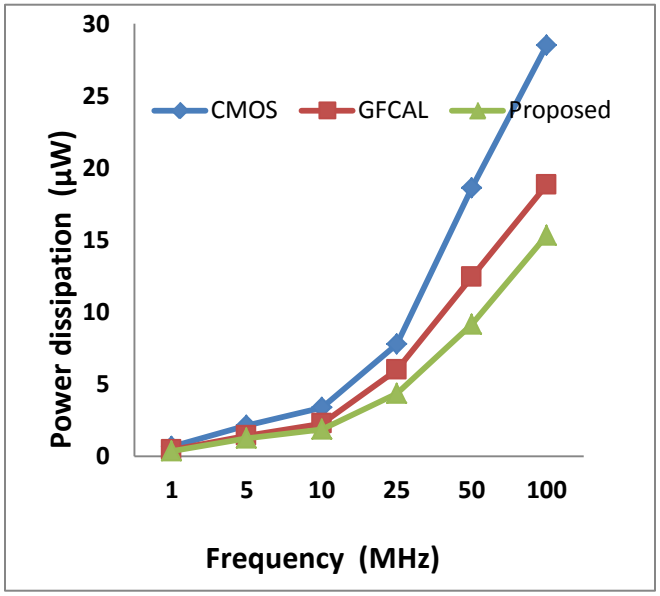


Figure 9 Power dissipation of Full adder circuit

Here we check the performance of the proposed full adder, GFCAL full adder and conventional CMOS full adder. The circuit is simulated using VIRTUOSO SPECTRE circuit simulator of cadence EDA tools. The length and width of the transistor are 180 nm and 240 nm, respectively the value of load capacitance is 5 fF. We have been simulated their power dissipation and compared with the variation in transition frequency. From the simulation result we find that power dissipation in proposed full adder is about 50% compare with that of the CMOS full adder.

5 Conclusions

In this paper we have presented energy efficient adiabatic logic circuits in which power delay product is improved more than 50% compared with that of conventional CMOS circuits. The simulation result and comparative performance revealed that power dissipation in proposed logic are considerably lower than conventional CMOS logic. Previously adiabatic logic circuits use of diode which limit the direction of current. It is not only difficult to fabricate diodes in CMOS technology but also consume more power. In this circuit, input and output logic levels are approximately same so it can be used in building hierarchical circuits. Further, the proposed circuits have low power density on chip and thus it can be used in power aware high performance VLSI circuitry.

REFERENCES

[1] K. Roy, S. Mukhopadhyay and H. mahmoodi-Meimand, "A leakage current mechanism and leakage reduction techniques in deep sub-micrometer CMOS circuits," Proc. IEEE, Vol.91, Issue2, Feb, 2003, pp.305-327.

[2] Hu Jianping; Cen Lizhang; Liu Xiao; " A new type of low power adiabatic circuit with complementary pass-transistor logic" ASIC,2003. Proc. 5th international Conference on Vol.2, Oct.2003, pp.1235-1238.

[3] K.A.Valiev and V.I. Starosel' ski, "A model and properties of a thermodynamically reversible logic gate" Mikroelektronika, 29(2), 83-98(2000).

[4] Kramer A.Denker J.S., Flower B., Moroney J., "Second-order adiabatic computation with 2N-2P and 2N-2N-2P logic circuit". Proc. Intern. Symp. Low power design, 1995, pp. 191-196.

[5] Moon Y., Jeong D.K., "An efficient charge recovery logic circuits". IEEE Journal of Solid-State Circuits, 1996, SC-31, (4) pp.514-522.

[6] Liu F., Lau K.T., "Pass transistor adiabatic logic with NMOS pull-down configuration", Electron. Lett., 1998, 34, (8) pp.739-741.

[7] Maksimovic D., Oklobdzija V.G., Nikolic B., Current K.W., "Clocked CMOS adiabatic logic with integrated single phase power clock supply". IEEE Transaction on very large scale integration system, 2000, 8,(4), pp.460-463.

[8] Younis S., Knight T., "Asymptotically zero energy split level charge recovery logic". Proc. Workshop on low power design, Napa Valley, California, 1994, pp. 177-182.

[9] Dickinson A.g., Denker J.S., "Adiabatic dynamic logic", IEEE Journal of Solid State Circuits, 1995, 30,(3), pp.311-315.

[10] Antonio B., Saletti R., "Ultra low power adiabatic circuit semi-custom design", IEEE Transaction on very large scale integration Systems, 2004,12, (11), pp. 1248-1253.

[11] N.S.S. Reddy, M .Satyam, and K.L. Kishore, " Caacadable adiabatic logic circuits for low power applications" IET circuit, Devices & System, 2(6), 518-526(2008).

[12] Nazarul Anuar, Yashuhiro Takahashi, and Toshikazu Sekine, "LSI implementation of a low power 4x4 bit array two phase clocked adiabatic static CMOS logic multiplier" Microelectronics Journal, Elsevier,43,244-249(2012).

[13] Wang Pengjun and Yu Junjun, " Design of two phase sinusoidal power clock and clocked transmission gate adiabatic logic circuit" Journal of Electronics (China), 24(2). 225-231(2007).

[14] A. Blotti, R. Saletti, "Ultralow power adiabatic circuit semi custom design" IEEE Transaction on VLSI system, 12(11), 1248-1253(2004).

[15] Nazarul Anuar, Yashuhiro Takahashi, and Toshikazu Sekine, " Two phase clock adiabatic static CMOS logic and its logic family" Journal of semiconductor technology and science, 10(1),1-10(2010).